IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re the Application of: Bu et al. | Docket No.: TI-36637

Serial No.: 10/810,905 | Art Unit: 2823

Filed: 03/26/2004 | Examiner: Stark, J. J.

Confirmation No.: 9390

Title: Improved CMOS Transistors and Methods of Forming Same

APPELLANTS' BRIEF

December 14, 2009

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Commissioner:

In response to the final Office Action, dated 05/26/20098, and the Notice of Appeal, dated 10/23/09, the Appellants submit this Appellants' Brief. The Commissioner is hereby requested and authorized to charge any required fees for the filing of this document to the deposit account of Texas Instruments Incorporated, Account No. 20-0668.

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REAL PARTY IN INTEREST

The Real Party in Interest in the present appeal is Texas Instruments Incorporated, the assignee, as evidenced by the assignment set forth at Reel 015157, Frame 0279.

RELATED APPEALS AND INTERFERENCES

The divisional case was appealed and subsequently abandoned. The BPAI affirmed the Examiner's rejections of Claims 11-18 in its decision dated 6-24-2009. The application number of the divisional case is 11/372,430 and it was filed 03-09-2006. Jarrett J. Stark was also the Examiner for the divisional application. In accordance with 37 C.F.R. 41.37(c) (1) (ii) and 37 C.F.R. 41.37(c) (1) (x), a copy of the decision dated 6-24-2009 is included in the section titled Related Proceedings Appendix.

STATUS OF CLAIMS

Claims 1-10 and 19-20 are the subject of this appeal. Claims 1-20 are pending, Claims 1-10 and 19-20 are rejected, and Claims 11-18 are withdrawn from consideration.

STATUS OF AMENDMENTS

The Appellants filed an amendment, dated June 5, 2006, in response to the non-final Office Action dated March 28, 2006. The Appellants filed an amendment, dated September 13, 2006, in response to the final Office Action dated July 12, 2006.

The Appellants filed a Request for Continued Examination on October 9, 2006 in response to the Advisory Action dated September 28, 2006.

The Appellants filed an amendment, dated January 30, 2007, in response to the non-final Office Action dated October 31, 2006. The Appellants filed an amendment, dated June 28, 2007, in response to the non-final Office Action dated April 3, 2007. The Appellants filed an amendment, dated September 8, 2007, in response to the final Office Action dated August 8, 2007.

The Appellants filed a Request for Continued Examination on October 4, 2007 in response to the Advisory Action dated September 21, 2007.

The Appellants filed an amendment, dated February 26, 2008, in response to the non-final Office Action dated December 31, 2007. The Appellants filed an Appeal Brief in response to the final Office Action dated April 30, 2008.

The Appellants filed an amendment, dated March 4, 2009, in response to the non-final Office Action dated December 12, 2008. The Appellants file this Appeal Brief in response to the final Office Action dated May 26, 2009.

SUMMARY OF THE CLAIMED SUBJECT MATTER

Independent Claim 1 is directed to a method for fabricating a CMOS transistor structure (FIGS. 2a-2d; page 3 line 4 through page 10 line 20). The method includes providing a semiconductor substrate (element 10 of FIGS. 2a-2d; page 4 lines 21-23 (paragraph 0015)) having an P-type dopant region to support an N-channel transistor of the CMOS transistor structure (page 4 line 25 through page 5 line 2 (paragraph 0015)) and a N-type dopant region to support a P-channel transistor of the CMOS transistor structure (page 4 line 25 through page 5 line 2 (paragraph 0015)), each of the N-type dopant and P-type dopant regions having an overlying gate stack (page 5 lines 4-15 (paragraph 0016)) including a conductive gate structure (element 30 of FIGS. 2a-2d; page 5 lines 4-15 (paragraph 0016)) and a dielectric gate structure (element 20 of FIGS. 2a-2d; page 5 lines 4-15 (paragraph 0016)). The method also includes forming lightly-doped extension regions in the semiconductor substrate adjacent each gate stack (element 100 of FIGS. 2b-2d, page 5 line 17 through page 6 line 11 (paragraphs 0017-0019)), depositing a layer of insulating material (element 110 of FIGS. 2c-2d; page 6 lines 21-29 (paragraph 0021)) in contact with a total exposed surface of the lightly-doped extension regions (FIGS. 2c-2d; page 6 line 12 through page 7 line 16, page 9 lines 21-28 (paragraphs 0020-0024 and 0033)), and forming an interfacial layer of nitrogen (element 112 of FIGS. 2c-2d; page 6 line 12 through page 7 line 16, page 9 lines 7-20 (paragraphs 0020-

0024, 0032)) below the layer of insulating material (page 6 lines 12-29, page 9 lines 7-20 (paragraphs 0020-0021 and 0032)) and within the total exposed surface of the lighted-doped extension regions (page 6 lines 12-29, page 9 lines 7-20 (paragraphs 0020-0021,0032)). In addition, the method includes forming at least one sidewall layer coupled to the layer of insulating material (page 6 lines 12-20, page 7 line 17 through page 8 line 5 (paragraphs 0020 and 0025-0026)), and forming source and drain regions (element 140 of FIG. 2d; page 8 lines 5-11 (paragraph 0027)) in the semiconductor substrate adjacent to each of the gate stacks. Furthermore, the method includes forming a capping layer (element 132 of FIG. 2d; page 8 line 11 through page 9 line 20 (paragraphs 0028-0032)) of contiguous silicon nitride over the semiconductor substrate (page 8 lines 11-18 (paragraph 0028)). Moreover, the method includes annealing (page 8 lines 18 through page 9 line 20 (paragraphs 0029-0032)), after the formation of the capping layer and with the capping layer in place (page 8 lines 18 through page 9 line 20 (paragraphs 0029-0032)), the extension regions and the source and drain regions (page 8 lines 18 through page 9 line 20 (paragraphs 0029-0032)), and removing all of the capping layer after the annealing (page 8 lines 23-28 (paragraph 0030)).

Claim 2 is dependant on Claim 1 and further specifies that the extension regions for the PMOS transistors have a dopant concentration in the range of about 1-2 e20 atoms/cm3 (page 11 lines 28-29, original Claim 2).

Claim 3 is dependant on Claim 1 and further specifies that the source and drain regions for the PMOS transistors have a dopant concentration in the range of about 1-2 e20 atoms/cm3 (page 12 lines 1-2, original Claim 3).

Claim 4 is dependant on Claim 1 and further specifies that the interfacial nitride layer has an atomic nitrogen concentration in the range of 2-15 atomic percent (page 6 lines 11-20 (paragraph 0020)).

Claim 5 is dependant on Claim 1 and further specifies that the insulating layer is selected from the group comprising silicon nitride and silicon oxide (page 6 lines 11-20, page 7 lines 16-28 (paragraphs 0020, 0025)).

Claim 6 is dependant on Claim 1 and further specifies that the step of forming an interfacial layer of nitrogen is performed using one of the methods selected from the group comprising an NH_3 thermal annealing (page 6 lines 20-29 (paragraph 0021)), an NH_3 or N_2 plasma treatment (page 7 lines 12-16 (paragraph 0024)), or an N implantation (page 7 lines 12-16 (paragraph 0024)).

Claim 7 is dependant on Claim 1 and further specifies that the capping layer has a thickness in the range of 200-1000 angstroms (page 8 lines 11-18 (paragraph 0028)).

Claim 8 is dependant on Claim 1 and further specifies that the annealing step is performed in the range of 1000-1100 degrees centigrade for a time in the range of less than about 10 seconds (page 8 lines 18-23 (paragraph 0029)).

Claim 9 is dependant on Claim 1 and further specifies that the gate stack further includes a nitride sidewall deposited with BTBAS precursor (page 7 lines 16-28 (paragraph 0025)).

Independent Claim 10 is directed to a method of fabricating a CMOS structure (FIG. 2d; page 3 line 28 through page 4 line 10, page 4 line 18 through page 10 line 20 (paragraphs 0011 and 0014-0037)). The method includes providing a semiconductor substrate (element 10 of FIGS. 2a-2d; page 4 line 21 through page 5 line 3 (paragraph 0015)) having an N-type dopant region to support a PMOS transistor of the CMOS transistor structure (page 4 line 21 through page 5 line 3 (paragraph 0015)) and a P-type dopant region to support an NMOS transistor of the CMOS transistor structure (page 4 line 21 through page 5 line 3 (paragraph 0015)), each of the N-type dopant and P-type dopant regions having an overlying gate stack (page 5 lines 3-16 (paragraph 0016)) including a conductive gate structure (element 30 of FIGS. 2a-2d; page 5 lines 3-16 (paragraph 0016)) and a dielectric gate structure (element 20 of FIGS. 2a-2d; page 5 lines 3-16 (paragraph 0016)). The method also includes forming lightly-

doped extension regions in the semiconductor substrate adjacent each gate stack (element 100 of FIGS. 2b-2d, page 5 line 16 through page 6 line 11 (paragraphs 0017-0019)), the lightly-doped extension regions in the N-type dopant region comprising a P-type dopant having a dopant concentration in the range of about 1-2 e20 atoms/cm3, depositing a layer of silicon oxide (element 110 of FIGS. 2c-2d; page 6 lines 21-29 (paragraph 0021)) in contact with a total exposed surface of the lightly-doped extension regions (FIGS. 2c-2d; page 6 line 11 through page 7 line 16, page 9 lines 20-28 (paragraphs 0020-0024 and 0033)), and forming an interfacial layer of nitrogen (element 112 of FIGS. 2c-2d; page 6 line 11 through page 7 line 16 (paragraphs 0020-0024)) below the layer of silicon oxide (page 6 lines 12-29, page 9 lines 7-20 (paragraphs 0020-0021 and 0032)) and within the total exposed surface of the lighted-doped extension regions (page 6 lines 11-20 (paragraph 0020)) where the interfacial layer of nitrogen has an atomic nitrogen concentration in the range of 2-15 atomic percent (page 6 lines 11-20 (paragraph 0020)). In addition, the method includes forming at least one sidewall layer coupled to the layer of insulating material (page 7 line 16 through page 8 line 5 (paragraphs 0025-0026)), forming source and drain regions (element 140 of FIG. 2d; page 8 lines 5-11 (paragraph 0027)) in the semiconductor substrate adjacent to each of the gate stacks where the source and drain regions in the N-type dopant region comprise a P-type dopant having a concentration in the range of about 1-2 e20 atoms/cm3. Furthermore, the method includes forming a capping layer (element 132 of FIG. 2d; page 8 line

11 through page 9 line 20 (paragraph 0028-0032)) of contiguous silicon nitride having a thickness in the range of about 200-1000 angstroms (page 8 lines 11-18 (paragraph 0028)). Moreover, the method includes annealing (page 8 lines 18-23 (paragraph 0029)), after the formation of the capping layer and with the capping layer in place, the extension regions and the source and drain regions at a temperature in the range of 1000-1100 degrees centigrade for a period in the range of less than about 10 seconds (page 8 lines 18-23 (paragraph 0029)), and removing all of the nitride cap after the annealing (page 8 lines 23-28 (paragraph 0030)).

Claim 19 is dependant on Claim 1 and further specifies that the steps of forming the layer of insulating material and forming the interfacial layer of nitrogen are performed without breaking vacuum (page 7 lines 6-12 (paragraph 0023)).

Claim 20 is dependant on Claim 10 and further specifies that the steps of forming the layer of insulating material and forming the interfacial layer of nitrogen are performed without breaking vacuum (page 7 lines 6-12 (paragraph 0023)).

GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

1. Claim 1 stands rejected under 35 U.S.C. §103(a) as unpatentable over the patent granted to Ahmad (U.S. Pat. No. 6,037,639) in view of the patent publication of Chen et al. (U.S. Pat. Pub. No. 2005/0136583 A1).

2. Claims 2-10 and 19-20 stand rejected under 35 U.S.C. §103(a) as unpatentable over the patent granted to Ahmad (U.S. Pat. No. 6,037,639) in view of the patent publication of Chen et al. (U.S. Pat. Pub. No. 2005/0136583 A1) and further in view of the patent publication of Wieczorek et al. (U.S. Pat. Pub. No. 2004/0061228 A1).

ARGUMENT

Rejection of Claim 1 under 35 U.S.C. §103(a) as unpatentable over the patent granted to Ahmad (U.S. Pat. No. 6,037,639) in view of the patent publication of Chen et al. (U.S. Pat. Pub. No. 2005/0136583 A1).

Claim 1

Independent Claim 1 positively recites depositing a layer of insulating material in contact with a total exposed surface of the lightly-doped extension regions. Claim 1 also positively recites forming an interfacial layer of nitrogen below the layer of insulating material and within the total exposed surface of the lightly-doped extension regions. In addition, Claim 1 positively recites removing all of the capping layer after the annealing. These advantageously claimed features are neither taught nor suggested by the patent granted to Ahmad or the patent publication of Chen et al.

The Appellants respectfully traverse the statements in the Office Action (page 3) that FIG. 2 of Ahmad teaches the formation of lightly-doped extension regions. The Appellants submit that element 118 of FIG. 2 is the amorphous ion implant area (column 3 lines 48-67), but not an implantation of arsenic or

phosphorous that is needed for the lightly-doped extension regions (column 3 lines 36-41).

Ahmad does not teach the advantageously claimed invention because Ahmad does not teach depositing a layer of insulating material in contact with a total exposed surface of the lightly-doped extension regions (column 4 lines 16-60). Ahmad teaches the formation of an oxide layer over the source/drain region (column 4 line 18) but not in contact with a total exposed surface of the lightly-doped extension region as advantageously claimed. In addition, Chen et al. does not teach the advantageously claimed invention because Chen et al. does not teach depositing a layer of insulating material in contact with a total exposed surface of the lightly-doped extension regions (paragraphs 0010-0012). Therefore, the combination of Ahmad and Chen et al. also does not teach the advantageously claimed step of depositing a layer of insulating material in contact with a total exposed surface of the lightly-doped extension regions.

Furthermore, Ahmad teaches the growth of an oxide layer 130 (column 4 lines 16-60) instead of the deposition of an insulating material as advantageously claimed. The Appellants respectfully traverse the unsupported assertion in the Office Action (page 4) that "Growing is a widely accepted functional equivalent to "depositing" when forming silicon oxide layers." The Appellants submit that the thermal oxidation process taught by Ahmad is required to achieve Ahmad's goal of

silicon-nitrogen "reaction" (column 4 lines 44-56), but Ahmad's growth process also carries the significant penalty of a high thermal budget (column 4 lines 32-41) that lowers the manufacturing yield. Therefore, growth and deposition processes are not interchangeable.

The Appellants respectfully traverse the unsupported assertion in the Office Action (bottom of page 3 and middle of page 4) that the insulating material is element 136 of Ahmad. The Appellants submit that Claim 1 defines the insulating material as having contact with the total exposed surface of the lightly-doped extension regions but element 136 in Ahmad has the width of a sidewall spacer (column 5 lines 15-16; FIG. 4) and therefore does not have contact with the total exposed surface of the lightly-doped extension regions.

The Appellants respectfully traverse the unsupported assertion in the Office Action (page 6) "Chen et al. discloses all of the claimed limitations except for the step of implanting a interfacial layer of nitrogen." The Appellants submit that the Office Action does not document the teaching in Chen et al. of depositing a layer of insulating material in contact with a total exposed surface of the lightly-doped extension regions (note that the Appellants' claimed insulating material is a different element than the Appellants' claimed capping layer). The Appellants also submit that the Office Action does not document the teaching in Chen et al. of the

advantageously claimed step of forming at least one sidewall layer coupled to the layer of insulating material.

Ahmad also does not teach the advantageously claimed invention because Ahmad does not teach forming an interfacial layer of nitrogen below the layer of insulating material and within the total exposed surface of the lightly-doped extension regions. Rather, Ahmad teaches the formation of the ion implanted area 118 "in source/drain regions" (column 3 line 53) and silicon nitride layer 131 "over the implanted source/drain regions" (column 4 line 55), instead of within the total exposed surface of the lightly-doped extension regions as advantageously claimed. In addition, Chen et al. does not teach the advantageously claimed invention because Chen et al. does not teach forming an interfacial layer of nitrogen below the layer of insulating material and within the total exposed surface of the lightly-doped extension regions (paragraphs 0010-0012). Therefore, the combination of Ahmad and Chen et al. also does not teach the advantageously claimed step of forming an interfacial layer of nitrogen below the layer of insulating material and within the total exposed surface of the lightly-doped extension regions.

Moreover, Ahmad teaches away from the advantageously claimed step of removing all of the capping layer after the annealing. Ahmad teaches that the cap layer must remain over the semiconductor substrate in order to block undesirable diffusion during a subsequent processing step (column 5 lines 44-50). Similarly,

Chen et al. teaches away from the advantageously claimed step of removing all of the capping layer after the annealing. Chen et al. teaches that portions of the cap layer must remain over the semiconductor substrate in order to serve as a resistant protection layer for subsequent CMOS processes (paragraphs 0021 and 0055-0056). Therefore, the combination of Ahmad and Chen et al. also teaches away from the advantageously claimed step of removing all of the capping layer after the annealing.

The Appellants traverse the assertion (on page 6 of the Office Action) that "It would have been within the scope of one of ordinary skill in the art at the time of the invention to combine the teachings of Ahmad and Chen". The Appellants submit that one of ordinary skill in the art would not combine a method requiring the cap layer to remain (Ahmad) with a method requiring the removal of portions of the cap layer (Chen et al.).

Therefore, Claim 1 is patentable over Ahmad and Chen et al.

Rejection of Claims 2-10 and 19-20 under 35 U.S.C. §103(a) as unpatentable over the patent granted to Ahmad (U.S. Pat. No. 6,037,639) in view of the patent publication of Chen et al. (U.S. Pat. Pub. No. 2005/0136583 A1) and further in view of the patent publication of Wieczorek et al. (U.S. Pat. Pub. No. 2004/0061228 A1).

Claim 2

Claim 2 is dependent on Claim 1 and is therefore allowable for the same reasons that Claim 1 is allowable. Furthermore, Claim 2 is allowable on its own merits because it recites additional features of the invention that, in combination with the limitations of Claim 1, are neither taught nor suggested by the patent granted to Ahmad nor the patent publications of Wieczorek et al. and Chen et al. Namely, Claim 2 further specifies the additional limitation that the extension regions for the PMOS transistors have a dopant concentration in the range of about 1-2 e20 atoms/cm3.

The Appellants respectfully traverse the assertion (on page 7 of the Office Action) that Wieczorek et al. teaches the dopant concentration of the extension regions in paragraph 0034. The Appellants submit that paragraph 0034 of Wieczorek et al. is directed to the concentration of the barrier diffusion material; however, the barrier diffusion is a different element than the extension regions

(note that the extension regions do not exist at the manufacturing step described in paragraph 0034 (corresponding to FIG. 2b) – rather, the extension regions are formed in paragraph 0037 (element 205 of FIG. 2c)).

Therefore, Claim 2 is patentable over Wieczorek et al., Ahmad, and Chen et al.

Claim 3

Claim 3 is dependent on Claim 1 and is therefore allowable for the same reasons that Claim 1 is allowable. Furthermore, Claim 3 is allowable on its own merits because it recites additional features of the invention that, in combination with the limitations of Claim 1, are neither taught nor suggested by the patent granted to Ahmad nor the patent publications of Wieczorek et al. and Chen et al. Namely, Claim 3 further specifies the additional limitation that the source and drain regions for the PMOS transistors have a dopant concentration in the range of about 1-2 e20 atoms/cm3.

The Appellants respectfully traverse the assertion (on page 7 of the Office Action) that Wieczorek et al. teaches the dopant concentration of the source and drain regions in paragraph 0034. The Appellants submit that paragraph 0034 of Wieczorek et al. is directed to the concentration of the barrier diffusion material;

however, the barrier diffusion is a different element than the source and drain regions (note that the source and drain regions do not exist at the manufacturing step described in paragraph 0034 (corresponding to FIG. 2b) – rather, the source and drain regions are formed in paragraph 0037 (element 204 of FIG. 2c)).

Therefore, Claim 3 is patentable over Wieczorek et al., Ahmad, and Chen et al.

Claim 4

Claim 4 is dependent on Claim 1 and is therefore allowable for the same reasons that Claim 1 is allowable. Furthermore, Claim 4 is allowable on its own merits because it recites additional features of the invention that, in combination with the limitations of Claim 1, are neither taught nor suggested by the patent granted to Ahmad nor the patent publications of Wieczorek et al. and Chen et al. Namely, Claim 4 further specifies the additional limitation that the interfacial nitride layer has an atomic nitrogen concentration in the range of 2-15 atomic percent.

The Appellants respectfully traverse the assertion (on page 8 of the Office Action) that in column 4 lines 8-15 Ahmad teaches the advantageously claimed interfacial nitride layer having an atomic nitrogen concentration in the range of 2-15 atomic percent. The Appellants submit that in column 4 line 13 Ahmad teaches

nitrogen concentration in the range of $1x10^{12}$ atoms to $1x10^{13}$ atoms. Therefore, Ahmad teaches a concentration of 0.005 to 0.5 atomic percent – a concentration range that is grossly insufficient for reducing the junction depth of the extensions during the high temperature anneal by retarding boron lateral diffusion (without degrading the active dopant concentration – for lower parasitic resistance; see paragraphs 0019-0020 of the Specification).

In addition, Wieczorek et al. does not teach the atomic nitrogen concentration of the interfacial nitride layer (paragraph 0034). Chen et al. also does not teach an atomic nitrogen concentration of an interfacial nitride layer (paragraph 0012). Therefore, the combination of Ahmad, Wieczorek et al. and Chen et al. also does not teach the advantageously claimed atomic nitrogen concentration of an interfacial nitride layer in the range of 2-15 atomic percent.

Therefore, Claim 4 is patentable over Wieczorek et al., Ahmad, and Chen et al.

Claim 5

Claim 5 is dependent on Claim 1 and is therefore allowable for the same reasons that Claim 1 is allowable. Furthermore, Claim 5 is allowable on its own merits because it recites additional features of the invention that, in combination with

the limitations of Claim 1, are neither taught nor suggested by the patent granted to Ahmad nor the patent publications of Wieczorek et al. and Chen et al. Namely, Claim 5 further specifies the additional limitation that the insulting layer is selected from the group comprising silicon nitride and silicon oxide.

Ahmad does not teach depositing a layer of insulating material selected from the group comprising silicon nitride and silicon oxide in contact with a total exposed surface of the lightly-doped extension regions (column 4 lines 16-20 and 43-56; note that the oxide layer 130 is grown and not deposited). Chen et al. also does not teach depositing a layer of insulating material selected from the group comprising silicon nitride and silicon oxide in contact with a total exposed surface of the lightly-doped extension regions (FIGS. 3-5 and 7; paragraphs 0034 and 0062). In addition, Wieczorek et al. does not teach depositing a layer of insulating material selected from the group comprising silicon nitride and silicon oxide in contact with a total exposed surface of the lightly-doped extension regions (FIGS. 1a and 2c; paragraphs 0012 and 0039). Therefore, the combination of Ahmad, Wieczorek et al. and Chen et al. also does not teach depositing a layer of insulating material selected from the group comprising silicon nitride and silicon oxide in contact with a total exposed surface of the lightly-doped extension regions.

The Appellants respectfully traverse the assertion in the Office Action (page 9) that element 126 of Ahmad is the advantageously claimed layer of insulating material in contact with a total exposed surface of the lightly-doped extension regions. The Appellants submit that element 126 is a sidewall (column 4 lines 20-21); therefore, it cannot be in contact with a total exposed surface of the lightly-doped extension regions as advantageously claimed.

Therefore, Claim 5 is patentable over Wieczorek et al., Ahmad, and Chen et al.

Claim 6

Claim 6 is dependent on Claim 1 and is therefore allowable for the same reasons that Claim 1 is allowable. Furthermore, Claim 6 is allowable on its own merits because it recites additional features of the invention that, in combination with the limitations of Claim 1, are neither taught nor suggested by the patent granted to Ahmad nor the patent publications of Wieczorek et al. and Chen et al. Namely, Claim 6 further specifies the additional limitation that the step of forming an interfacial layer of nitrogen is performed using one of the methods selected from the group comprising an NH_3 thermal annealing, an NH_3 or N_2 plasma treatment, or an N implantation.

Wieczorek et al. does not teach forming an interfacial layer of nitrogen using one of the methods selected from the group comprising an NH_3 thermal annealing or an NH_3 or N_2 plasma treatment (paragraph 0034). Chen et al. does not teach forming an interfacial layer of nitrogen using one of the methods selected from the group comprising an NH_3 thermal annealing or an NH_3 or N_2 plasma treatment (paragraphs 0010-0012). Ahamd does not teach forming an interfacial layer of nitrogen using one of the methods selected from the group comprising an NH_3 thermal annealing or an NH_3 or N_2 plasma treatment (column 4 lines 8-15). Therefore, the combination of Wieczorek et al., Chen et al. and Ahmad also does not teach forming an interfacial layer of nitrogen using one of the methods selected from the group comprising an NH_3 thermal annealing or an NH_3 or N_2 plasma treatment.

The Appellants respectfully traverse the assertion in the Office Action (page 9) that Ahmad teaches forming an interfacial layer of nitrogen using one of the methods selected from the group comprising an NH_3 thermal annealing or an NH_3 or N_2 plasma treatment in FIG. 3, column 1 line 66 to column 2 line 11, and column 2 lines 44-61. The Appellants submit that neither NH_3 thermal annealing nor NH_3 or N_2 plasma treatment are taught in the cited sections of Ahmad.

Therefore, Claim 6 is patentable over Wieczorek et al., Ahmad, and Chen et al.

Claim 7

Claim 7 is dependent on Claim 1 and is therefore allowable for the same reasons that Claim 1 is allowable. Furthermore, Claim 7 is allowable on its own merits because it recites additional features of the invention that, in combination with the limitations of Claim 1, are neither taught nor suggested by the patent granted to Ahmad nor the patent publications of Wieczorek et al. and Chen et al. Namely, Claim 7 further specifies the additional limitation that the capping layer has a thickness in the range of 200-1000 angstroms.

Neither Ahmad (column 5 lines 44-50), Wieczorek et al. (paragraphs 0036-0037), nor Chen et al. (paragraphs 0055-0056) teach the steps of forming a capping layer having a thickness in the range of 200-1000 angstroms and then removing the capping layer after the annealing - as required by the combination of Claims 1 and 7 – therefore, the combination of Ahmad, Wieczorek et al. and Chen et al. also does not teach the advantageously claimed steps of forming a capping layer having a thickness in the range of 200-1000 angstroms and then removing the capping layer after the annealing.

Therefore, Claim 7 is patentable over Ahmad, Wieczorek et al. and Chen et al.

Claim 8

Claim 8 is dependent on Claim 1 and is therefore allowable for the same reasons that Claim 1 is allowable. Furthermore, Claim 8 is allowable on its own merits because it recites additional features of the invention that, in combination with the limitations of Claim 1, are neither taught nor suggested by the patent granted to Ahmad nor the patent publications of Wieczorek et al. and Chen et al. Namely, Claim 8 further specifies the additional limitation that the annealing step is performed in the range of 1000-1100 degrees centigrade for a time in the range of less than about 10 seconds.

Neither Ahmad (column 5 lines 44-50), Wieczorek et al. (paragraphs 0036-0037), nor Chen et al. (paragraphs 0055-0056) teach the steps of annealing in the range of 1000-1100 degrees centigrade for a time in the range of less than about 10 seconds and then removing all of the capping layer after the annealing - as required by the combination of Claims 1 and 8 - therefore, the combination of Ahmad, Wieczorek et al., and Chen et al. also does not teach the advantageously claimed steps of annealing in the range of 1000-1100 degrees centigrade for a time in the range of less than about 10 seconds and then removing all of the capping layer after the annealing.

Therefore, Claim 8 is patentable over Ahmad, Wieczorek et al., and Chen et al.

Claim 9

Claim 9 is dependent on Claim 1 and is therefore allowable for the same reasons that Claim 1 is allowable. Furthermore, Claim 9 is allowable on its own merits because it recites additional features of the invention that, in combination with the limitations of Claim 1, are neither taught nor suggested by the patent granted to Ahmad nor the patent publications of Wieczorek et al. and Chen et al. Namely, Claim 9 further specifies the additional limitation that the step of forming at least one sidewall layer includes the use of a BTBAS precursor.

The Appellants respectfully traverse the assertion (on page 10 of the Office Action) that Chen et al. specifies in paragraph 0046 the precursor that is used in the step of forming a sidewall layer. The Appellants submit that paragraph 0046 of Chen et al. is directed to the precursor used during the formation of the capping layer 24 (see paragraph 0042) but not the formation of the sidewall spacer 16.

Because neither Ahmad (column 5 lines 13-21), Wieczorek et al. (paragraph 0036), nor Chen et al. (paragraph 0028) teach forming at least one

sidewall layer using a BTBAS precursor, the combination of Ahmad, Wieczorek et al. and Chen et al. also does not teach the advantageously claimed step of forming at least one sidewall layer using a BTBAS precursor.

Therefore, Claim 9 is patentable over Ahmad, Wieczorek et al., and Chen et al.

Claim 10

Independent Claim 10 positively recites depositing a layer of silicon oxide in contact with a total exposed surface of the lightly-doped extension regions. Claim 10 also positively recites forming an interfacial layer of nitrogen below the layer of silicon oxide and within the total exposed surface of the lightly-doped extension regions. In addition, Claim 10 positively recites removing all of the nitride cap after the annealing. These advantageously claimed features are neither taught nor suggested by the patent granted to Ahmad or the patent publications of Chen et al. and Wieczorek et al.

The Appellants respectfully traverse the statements in the Office Action (page 11) that FIG. 2 of Ahmad teaches the formation of lightly-doped extension regions. The Appellants submit that element 118 of FIG. 2 is the amorphous ion implant area (column 3 lines 48-67), but not an implantation of arsenic or

phosphorous that is needed for the lightly-doped extension regions (column 3 lines 36-41). The Appellants also respectfully traverse the statements in the Office Action (page 15) that Wieczorek et al. teaches the dopant concentration of the extension regions in paragraph 0034. The Appellants submit that paragraph 0034 of Wieczorek et al. is directed to the concentration of the barrier diffusion material; however, the barrier diffusion is a different element than the extension regions (note that the extension regions do not exist at the manufacturing step described in paragraph 0034 (corresponding to FIG. 2b) – rather, the extension regions are formed in paragraph 0037 (element 205 of FIG. 2c)).

Ahmad does not teach the advantageously claimed invention because Ahmad does not teach depositing a layer of silicon oxide in contact with a total exposed surface of the lightly-doped extension regions (column 4 lines 16-60). Ahmad teaches the formation of an oxide layer over the source/drain region (column 4 line 18) but not in contact with a total exposed surface of the lightly-doped extension region as advantageously claimed. In addition, Chen et al. does not teach the advantageously claimed invention because Chen et al. does not teach depositing a layer of silicon oxide in contact with a total exposed surface of the lightly-doped extension regions (paragraphs 0010-0012). In addition, Wieczorek et al. does not teach the advantageously claimed invention because Wieczorek et al. does not teach depositing a layer of silicon oxide in contact with a total exposed surface of the lightly-doped extension regions (FIGS. 1a and 2c; paragraphs 0012

and 0039). Therefore, the combination of Ahmad, Chen et al., and Wieczorek et al. also does not teach the advantageously claimed step of depositing a layer of silicon oxide in contact with a total exposed surface of the lightly-doped extension regions.

Furthermore, Ahmad teaches the growth of an oxide layer 130 (column 4 lines 16-60) instead of the deposition of silicon oxide as advantageously claimed. The Appellants respectfully traverse the unsupported assertion in the Office Action (page 11) that "Growing is a widely accepted functional equivalent to "depositing" when forming silicon oxide layers." The Appellants submit that the thermal oxidation process taught by Ahmad is required to achieve Ahmad's goal of silicon-nitrogen "reaction" (column 4 lines 44-56), but Ahmad's growth process also carries the significant penalty of a high thermal budget (column 4 lines 32-41) that lowers the manufacturing yield. Therefore, growth and deposition processes are not interchangeable.

The Appellants respectfully traverse the unsupported assertion in the Office Action (pages 11-12) that the insulating material is element 136 of Ahmad. The Appellants submit that Claim 10 defines the silicon oxide as having contact with the total exposed surface of the lightly-doped extension regions but element 136 in Ahmad has the width of a sidewall spacer (column 5 lines 15-16; FIG. 4) and therefore does not have contact with the total exposed surface of the lightly-doped extension regions.

Ahmad also does not teach the advantageously claimed invention because Ahmad does not teach forming an interfacial layer of nitrogen below the layer of insulating material and within the total exposed surface of the lightly-doped extension regions. Rather, Ahmad teaches the formation of the ion implanted area 118 "in source/drain regions" (column 3 line 53) and silicon nitride layer 131 "over the implanted source/drain regions" (column 4 line 55), instead of within the total exposed surface of the lightly-doped extension regions as advantageously claimed. In addition, Chen et al. does not teach the advantageously claimed invention because Chen et al. does not teach forming an interfacial layer of nitrogen below the layer of insulating material and within the total exposed surface of the lightly-doped extension regions (paragraphs 0010-0012). Furthermore, Wieczorek et al. does not teach the advantageously claimed invention because Wieczorek et al. does not teach forming an interfacial layer of nitrogen below the layer of insulating material and within the total exposed surface of the lightly-doped extension regions (paragraphs 0034 and 0036; note that the extension regions don't exist when the interfacial layer of nitrogen is formed). Therefore, the combination of Ahmad, Chen et al. and Wieczorek et al. also does not teach the advantageously claimed step of forming an interfacial layer of nitrogen below the layer of insulating material and within the total exposed surface of the lightly-doped extension regions.

The Appellants respectfully traverse the assertion (on page 13 of the Office Action) that in column 4 lines 8-15 Ahmad teaches the advantageously claimed interfacial nitride layer having an atomic nitrogen concentration in the range of 2-15 atomic percent. The Appellants submit that in column 4 line 13 Ahmad teaches nitrogen concentration in the range of $1x10^{12}$ atoms to $1x10^{13}$ atoms. Therefore, Ahmad teaches a concentration of 0.005 to 0.5 atomic percent – a concentration range that is grossly insufficient for reducing the junction depth of the extensions during the high temperature anneal by retarding boron lateral diffusion (without degrading the active dopant concentration – for lower parasitic resistance; see paragraphs 0019-0020 of the Specification).

The Appellants respectfully traverse the assertion (on page 15 of the Office Action) that Wieczorek et al. teaches the dopant concentration of the source and drain regions in paragraph 0034. The Appellants submit that paragraph 0034 of Wieczorek et al. is directed to the concentration of the barrier diffusion material; however, the barrier diffusion is a different element than the source and drain regions (note that the source and drain regions do not exist at the manufacturing step described in paragraph 0034 (corresponding to FIG. 2b) – rather, the source and drain regions are formed in paragraph 0037 (element 204 of FIG. 2c)).

Moreover, Ahmad teaches away from the advantageously claimed step of removing all of the nitride cap after the annealing. Ahmad teaches that the cap layer must remain over the semiconductor substrate in order to block undesirable diffusion during a subsequent processing step (column 5 lines 44-50). Similarly, Chen et al. teaches away from the advantageously claimed step of removing all of the nitride cap after the annealing. Chen et al. teaches that portions of the cap layer must remain over the semiconductor substrate in order to serve as a resistant protection layer for subsequent CMOS processes (paragraphs 0021 and 0055-0056). Furthermore, Wieczorek et al. teaches that the transistor element 200 should be formed without using a capping layer (paragraph 0038). Therefore, the combination of Ahmad, Chen et al., and Wieczorek et al. also teaches away from the advantageously claimed step of removing all of the nitride cap after the annealing.

The Appellants traverse the assertion (on page 13 of the Office Action) that "It would have been within the scope of one of ordinary skill in the art at the time of the invention to combine the teachings of Ahmad and Chen". The Appellants submit that one of ordinary skill in the art would not combine a method requiring the cap layer to remain (Ahmad) with a method requiring the removal of portions of the cap layer (Chen et al.).

Therefore, Claim 10 is patentable over Ahmad, Wieczorek et al., and Chen et al.

Claim 19

Claim 19 is dependent on Claim 1 and is therefore allowable for the same reasons that Claim 1 is allowable. Furthermore, Claim 19 is allowable on its own merits because it recites additional features of the invention that, in combination with the limitations of Claim 1, are neither taught nor suggested by the patent granted to Ahmad nor the patent publications of Wieczorek et al. and Chen et al. Namely, Claim 19 further specifies the additional limitation that the steps of forming the layer of insulating material and forming the interfacial layer of nitrogen are performed without breaking vacuum.

The Appellants respectfully traverse the assertion (on page 10 of the Office Action) that when the cited references fail to teach an advantageously claimed step that "the process is understood to be performed". The Appellants respectfully submit the Examiner has failed to establish a prima facie case of obviousness. (*Ex parte* Humphreys, 24 USPQ2d 1255, 1262.)

Ahmad does not teach forming a layer of insulating material in contact with a total exposed surface of the lightly-doped extension regions plus forming an

interfacial layer of nitrogen within the total exposed surface of the lightly-doped extension regions (column 2 lines 35-42); therefore, Ahmad cannot teach that the steps of forming the layer of insulating material and forming the interfacial layer of nitrogen are performed without breaking vacuum, as advantageously claimed. Wieczorek et al. does not teach forming a layer of insulating material in contact with a total exposed surface of the lightly-doped extension regions plus forming an interfacial layer of nitrogen within the total exposed surface of the lightly-doped extension regions (paragraphs 0032-0036; FIGS. 2a-2c); therefore, Wieczorek et al. cannot teach that the steps of forming the layer of insulating material and forming the interfacial layer of nitrogen are performed without breaking vacuum, as advantageously claimed. Similarly, Chen et al. does not teach forming a layer of insulating material in contact with a total exposed surface of the lightly-doped extension regions plus forming an interfacial layer of nitrogen within the total exposed surface of the lightly-doped extension regions (paragraphs 0024-0034; FIGS. 1-3); therefore, Chen et al. cannot teach that the steps of forming the layer of insulating material and forming the interfacial layer of nitrogen are performed without breaking vacuum, as advantageously claimed. Because neither Ahmad, Wieczorek et al., nor Chen et al. teach that the steps of forming the layer of insulating material and forming the interfacial layer of nitrogen are performed without breaking vacuum; the combination of Ahmad, Wieczorek et al., and Chen et al. also does not teach the advantageously

claimed steps of forming the layer of insulating material and forming the interfacial layer of nitrogen are performed without breaking vacuum.

Therefore, Claim 19 is patentable over Ahmad, Wieczorek et al. and Chen et al.

Claim 20

Claim 20 is dependent on Claim 10 and is therefore allowable for the same reasons that Claim 10 is allowable. Furthermore, Claim 20 is allowable on its own merits because it recites additional features of the invention that, in combination with the limitations of Claim 10, are neither taught nor suggested by the patent granted to Ahmad nor the patent publications of Wieczorek et al. and Chen et al. Namely, Claim 20 further specifies the additional limitation that the steps of forming the layer of silicon oxide and forming the interfacial layer of nitrogen are performed without breaking vacuum.

The Appellants respectfully traverse the assertion (on page 10 of the Office Action) that when the cited references fail to teach an advantageously claimed step that "the process is understood to be performed". The Appellants respectfully submit the Examiner has failed to establish a prima facie case of obviousness. (*Ex parte* Humphreys, 24 USPQ2d 1255, 1262.)

Ahmad does not teach forming a layer of insulating material in contact with a total exposed surface of the lightly-doped extension regions plus forming an interfacial layer of nitrogen within the total exposed surface of the lightly-doped extension regions (column 2 lines 35-42); therefore, Ahmad cannot teach that the steps of forming the layer of insulating material and forming the interfacial layer of nitrogen are performed without breaking vacuum, as advantageously claimed. Wieczorek et al. does not teach forming a layer of insulating material in contact with a total exposed surface of the lightly-doped extension regions plus forming an interfacial layer of nitrogen within the total exposed surface of the lightly-doped extension regions (paragraphs 0032-0036; FIGS. 2a-2c); therefore, Wieczorek et al. cannot teach that the steps of forming the layer of insulating material and forming the interfacial layer of nitrogen are performed without breaking vacuum, as advantageously claimed. Similarly, Chen et al. does not teach forming a layer of insulating material in contact with a total exposed surface of the lightly-doped extension regions plus forming an interfacial layer of nitrogen within the total exposed surface of the lightly-doped extension regions (paragraphs 0024-0034; FIGS. 1-3); therefore, Chen et al. cannot teach that the steps of forming the layer of insulating material and forming the interfacial layer of nitrogen are performed without breaking vacuum, as advantageously claimed. Because neither Ahmad, Wieczorek et al., nor Chen et al. teach that the steps of forming the layer of insulating material and forming the interfacial layer of

nitrogen are performed without breaking vacuum; the combination of Ahmad, Wieczorek et al., and Chen et al. also does not teach the advantageously claimed steps of forming the layer of insulating material and forming the interfacial layer of nitrogen are performed without breaking vacuum.

Therefore, Claim 20 is patentable over the patent publications of Wieczorek et al. and Chen et al.

CONCLUSION

For the reasons stated above, the Appellants respectfully contend that each claim is patentable. Therefore, the reversal of all rejections is courteously solicited.

Respectfully submitted,

/Rose Alyssa Keagy/

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CLAIMS APPENDIX

1. A method for fabricating a CMOS transistor structure, comprising the steps of:

providing a semiconductor substrate having a P-type dopant region to support an N-channel transistor of the CMOS transistor structure and an N-type dopant region to support a P-channel transistor of the CMOS transistor structure, each of the N-type dopant and P-type dopant regions having an overlying gate stack including a conductive gate structure and a dielectric gate structure;

forming lightly-doped extension regions in the semiconductor substrate adjacent each gate stack;

depositing a layer of insulating material in contact with a total exposed surface of the lightly-doped extension regions;

forming an interfacial layer of nitrogen below the layer of insulating material and within the total exposed surface of the lightly-doped extension regions;

forming at least one sidewall layer coupled to the layer of insulating material;

forming source and drain regions in the semiconductor substrate adjacent to each of the gate stacks;

forming a capping layer of contiguous silicon nitride over the semiconductor substrate;

annealing, after the formation of the capping layer and with the capping layer in place, the extension regions and the source and drain regions; and

removing all of the capping layer after the annealing.

2. The method of claim 1 wherein the extension regions for the PMOS transistors have a dopant concentration in the range of about 1-2 e20 atoms/cm3.

3. The method of claim 1 wherein the source and drain regions for the PMOS transistors have a dopant concentration in the range of about 1-2 e20 atoms/cm3.

4. The method of claim 1 wherein said interfacial nitride layer has an atomic nitrogen concentration in the range of 2-15 atomic percent.

5. The method of claim 1 wherein the insulting layer is selected from the group comprising silicon nitride and silicon oxide.

6. The method of claim 1 wherein the step of forming an interfacial layer of nitrogen is performed using one of the methods selected from the group comprising an NH_3 thermal annealing, an NH_3 or N_2 plasma treatment, or an N implantation.

7. The method of claim 1 wherein the capping layer has a thickness in the range of 200-1000 angstroms.

8. The method of claim 1 wherein the annealing step is performed in the range of 1000-1100 degrees centigrade for a time in the range of less than about 10 seconds.

9. The method of claim 1 wherein the step of forming at least one sidewall layer includes the use of a BTBAS precursor.

10. A method for fabricating a CMOS transistor structure, comprising the steps of:

providing a semiconductor substrate having an N-type dopant region to support an PMOS transistor of the CMOS transistor structure and a P-type dopant region to support a NMOS transistor of the CMOS transistor structure, each of the N-type dopant and P-type dopant regions having an overlying gate stack including a conductive gate structure and a dielectric gate structure;

forming lightly-doped extension regions in the semiconductor substrate adjacent each gate stack, the lightly-doped extension regions in the N-type dopant region comprising a P-type dopant having a dopant concentration in the range of about 1-2 e20 atoms/cm3;

depositing a layer of silicon oxide in contact with a total exposed surface of the lightly-doped extension regions;

forming an interfacial layer of nitrogen below the layer of silicon oxide and within the total exposed surface of the lightly-doped extension regions, the interfacial layer of nitrogen having an atomic nitrogen concentration in the range of 2-15 atomic percent;

forming at least one sidewall layer coupled to the layer of insulating material;

forming source and drain regions in the semiconductor substrate adjacent to each of the gate stacks, the source and drain regions in the in the N-type dopant region comprising a P-type dopant having a concentration in the range of about 1-2 e20 atoms/cm3;

forming a capping layer of contiguous silicon nitride having a thickness in the range of about 200-1000 angstroms over the semiconductor substrate;

annealing, after the formation of the capping layer and with the capping layer in place, the extension regions and the source and drain regions at a temperature in the range of 1000-1100 degrees centigrade for a period in the range of less than about 10 seconds; and

removing all of the nitride cap after the annealing.

19. The method of claim 1 wherein the steps of forming the layer of insulating material and forming the interfacial layer of nitrogen are performed without breaking vacuum.

20. The method of claim 10 wherein the steps of forming the layer of silicon oxide and forming the interfacial layer of nitrogen are performed without breaking vacuum.

EVIDENCE APPENDIX

None

RELATED PROCEEDINGS APPENDIX

In accordance with 37 C.F.R. 41.37(c)(1)(ii) and 37 C.F.R. 41.37(c)(1)(x), a copy of the BPAI decision dated 6-24-2009 regarding the divisional U.S. Patent Application Serial Number 11/372,430 is included immediately infra.

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UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

Ex parte HAOWEN BU, BRIAN HORNUNG, P. R. CHIDAMBARAM, AMITABH JAIN, RAJESH KHAMANKAR, NANDU MAHALINGAM, and SRINIVANSAN CHAKRAVARTHI

Appeal 2009-001621
Application 11/372,430[1]
Technology Center 2800

Decided:[2] June 22, 2009

Before MAHSHID D. SAADAT, MARC S. HOFF, and CARLA M. KRIVAK, *Administrative Patent Judges*.

HOFF, *Administrative Patent Judge*.

DECISION ON APPEAL

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[1] The real party in interest is Texas Instruments Incorporated.

[2] The two-month time period for filing an appeal or commencing a civil action, as recited in 37 C.F.R. § 1.304, begins to run from the decided date shown on this page of the decision. The time period does not run from the Mail Date (paper delivery) or Notification Date (electronic delivery).

STATEMENT OF CASE

Appellants appeal under 35 U.S.C. § 134(a) from a Final Rejection of claims 11-18.[3] We have jurisdiction under 35 U.S.C. § 6(b).

We affirm.

Appellants' invention relates to complementary metal oxide semiconductor (CMOS) transistor formation. Appellants form lightly-doped extension regions adjacent each transistor gate stack; form a layer of insulating material over the lightly-doped extension regions; and form an interfacial layer of nitrogen at the interface of the insulating layer and the lightly-doped extension regions. Appellants then form source and drain regions in the semiconductor substrate; form a capping layer of contiguous silicon nitride over the substrate and each of the gate stacks; anneal, with the capping layer in place, the extension and source and drain regions; and remove the capping layer after the annealing step (Spec. 3).

Claim 11 is exemplary:

11. A semiconductor structure formed in the process of fabricating a CMOS transistor structure prior to an activating anneal, comprising:

a semiconductor substrate having an P-type dopant region to support an NMOS transistor of the CMOS transistor structure and a N-type dopant region to support a PMOS transistor of the CMOS transistor structure, each of the N-type dopant and P-type dopant regions having an overlying gate stack including a conductive gate structure and a dielectric gate structure;

lightly-doped extension regions in the semiconductor substrate adjacent each gate stack;

a layer of insulating material over a total exposed surface of the lightly-doped extension regions;

an interfacial layer of nitrogen formed at the interface of the lighted-doped extension regions and the layer of insulating material;

[3] Claims 1-10 have been canceled.

source and drain regions in the semiconductor substrate adjacent to each of the gate stacks; and

a capping layer of contiguous silicon nitride over the semiconductor substrate and each of the gate stacks of the CMOS transistor structure.

The prior art relied upon by the Examiner in rejecting the claims on appeal is:

Guo	US 6,878,583 B2	Apr. 12, 2005

Claims 11, 12, 16, and 17 stand rejected under 35 U.S.C. § 102(e) as being anticipated by Guo.

Claims 13-15 and 18 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Guo.

Throughout this decision, we make reference to the Appeal Brief ("Br.," filed October 3, 2007) and the Examiner's Answer ("Ans.," mailed December 20, 2007) for their respective details.

ISSUES

Appellants argue that Guo does not teach a layer of insulating material, composed of silicon oxide, over a total exposed surface of the lightly-doped extension regions, nor an interfacial layer of nitrogen formed at the interface of the lightly-doped extension regions and the layer of insulating material, nor a capping layer of contiguous silicon nitride having a thickness of 200-1000 angstroms, nor a gate stack having a nitride sidewall deposited with a BTBAS precursor.

Appellants further argue that it would not have been obvious to modify Guo to include a dopant concentration for the extension regions, or the source and drain regions, in the range of about 1-2 e20 atoms/cm3, nor to

include an interfacial nitride layer with an atomic nitrogen concentration in the range of 2-15 atomic percent.

Appellants' arguments present us with the following issues:

1. Have Appellants shown that the Examiner erred in finding that Guo teaches: a layer of insulating material, composed of silicon oxide, over a total exposed surface of the lightly-doped extension regions; an interfacial layer of nitrogen formed at the interface of the lightly-doped extension regions and the layer of insulating material; a capping layer of contiguous silicon nitride having a thickness of 200-1000 angstroms; or a gate stack having a nitride sidewall deposited with a BTBAS precursor, as the claims require?

2. Have Appellants shown that the Examiner erred in finding that it would have been obvious to modify Guo to provide extension regions and source and drain regions with the dopant concentration claimed, or that the interfacial nitride layer should have an atomic nitrogen concentration in the range of 2-15 atomic percent?

FINDINGS OF FACT

The following Findings of Fact (FF) are shown by a preponderance of the evidence.

The Invention

1. According to Appellant, the invention concerns complementary metal oxide semiconductor (CMOS) transistor formation (Spec. 3).

Guo

2. Guo teaches an integration method to enhance gate activation in a CMOS device (col. 1, ll. 8-10).

3. Guo teaches dielectric spacers 16, made of an insulating material, that overlay a total exposed surface of the lightly-doped extension regions 18 (col. 3, ll. 25-26; Fig. 4).

4. The dielectric spacers are composed of silicon oxide (col. 3, ll. 25-26).

5. Guo teaches that the oxide of dielectric spacer 16, including the portion at the interface of the lightly-doped extension regions and the remaining insulating material, is subjected to thermal nitridation in a nitrogen-containing atmosphere (col. 3, ll. 30-33; Fig. 1).

6. Guo teaches that the thickness of cap dielectric film 22 is kept to approximately between 100 Å to 500 Å (col. 4, ll. 6-8). The cap dielectric film may be formed of silicon dioxide (col. 4, l. 4).

PRINCIPLES OF LAW

"A rejection for anticipation under section 102 requires that each and every limitation of the claimed invention be disclosed in a single prior art reference." *See In re Buszard*, 504 F.3d 1364, 1366 (Fed. Cir. 2007) (quoting *In re Paulsen*, 30 F.3d 1475, 1478-79 (Fed. Cir. 1994)). Anticipation of a claim requires a finding that the claim at issue reads on a prior art reference. *Atlas Powder Co. v. IRECO, Inc.*, 190 F.3d 1342, 1346 (Fed. Cir. 1999) (quoting *Titanium Metals Corp. v. Banner*, 778 F.2d 775, 781 (Fed. Cir. 1985)).

On the issue of obviousness, the Supreme Court has stated that "the obviousness analysis cannot be confined by a formalistic conception of the words teaching, suggestion, and motivation." *KSR Int'l Co. v. Teleflex Inc.*, 550 U.S. 398, 419 (2007). Further, the Court stated "[t]he combination of familiar elements according to known methods is likely to be obvious when

it does no more than yield predictable results." *Id.* at 416. "One of the ways in which a patent's subject matter can be proved obvious is by noting that there existed at the time of the invention a known problem for which there was an obvious solution encompassed by the patent's claims." *Id.* at 419-420.

"[W]here the general conditions of a claim are disclosed in the prior art, it is not inventive to discover the optimum or workable ranges by routine experimentation." *In re Aller*, 220 F.2d 454, 456 (CCPA 1955). "[R]outine experimentation within the teachings of the art is not patentable, even though some improvement may be obtained thereby." *In re Fay*, 347 F.2d 597, 600 (CCPA 1965)(internal citations omitted). A particular parameter must first be recognized as a result-effective variable, i.e., a variable which achieves a recognized result, before the determination of the optimum or workable ranges of said variable might be characterized as routine experimentation. *In re Antonie,* 559 F.2d 618, 620 (CCPA 1977). "[I]t is the patentability of the *product* claimed and *not* of the recited process steps which must be established." *In re Brown*, 459 F.2d 531, 535 (CCPA 1972). "[E]ven though *product-by-process claims are limited by and defined by the process,* determination of patentability is based on the product itself." *In re Thorpe,* 777 F.2d 695, 697 (Fed. Cir. 1985). "Where a product-by-process claim is rejected over a prior art product that appears to be identical, although produced by a different process, the burden is upon the applicant to come forward with evidence establishing an unobvious difference between the claimed product and the prior art product." *In re Marosi,* 710 F.2d 799, 803 (Fed. Cir. 1983).

ANALYSIS

CLAIM 11

Appellants argue that Guo does not anticipate claim 11 because Guo fails to teach a layer of insulating material over the total exposed surface of the lightly-doped extension regions; Guo fails to teach an interfacial layer of nitrogen formed at the interface; and Guo's gate element 14 cannot simultaneously meet the conductive gate structure of the gate stack, the interfacial layer of nitrogen, and the spacer sidewalls (Br. 12-13). We do not find Appellants' arguments persuasive of Examiner error.

Guo teaches dielectric spacers 16, made of an insulating material, that overlay a total exposed surface of the lightly-doped extension regions 18 (FF 3). Guo, thus, teaches the "layer of insulating material" recited.

We concur in the Examiner's finding that Guo teaches the claimed interfacial layer of nitrogen (Ans. 5). Guo teaches that the oxide of dielectric spacer 16, including the portion at the interface of the lightly-doped extension regions and the rest of the insulating material, is subjected to thermal nitridation in a nitrogen-containing atmosphere (FF 5), which will result in the presence of nitrogen at the interface (Ans. 11). We further concur in the Examiner's finding that the annealing process will inherently result in the formation of a nitrogen interfacial layer (Ans. 11). Therefore, we find that Guo teaches the claimed interfacial layer of (i.e., containing) nitrogen formed at the interface of the lightly-doped extension regions 18 and the layer of insulating material 16.

Finally, Appellants' argument that conductor gate 14 of Guo cannot simultaneously meet three elements of the claimed invention is not germane to the rejection at issue, because the Examiner does not rely on conductor

gate 14 to teach those limitations. We further observe that, contrary to Appellants' argument, "spacer sidewalls" are not recited in claim 11.

Therefore, because Appellants have not established error in the Examiner's position, we will sustain the Examiner's rejection of claim 11 under 35 U.S.C. § 102.

CLAIM 12

Appellants argue that Guo fails to anticipate the subject matter of claim 12 because Guo does not teach a silicon oxide insulating layer, pointing out that Guo's capping layer 22 is made of silicon nitride (Br. 15).

Appellants' argument is not persuasive of Examiner error. Guo teaches dielectric spacers 16 that are positioned so as to cover the total exposed surface of the lightly-doped extension regions (FF 3). The dielectric spacers are composed of silicon oxide (FF 4).

Therefore, because Appellants have not identified error in the Examiner's position, we will sustain the Examiner's rejection of claim 12 under 35 U.S.C. § 102.

CLAIM 16

Appellants argue that Guo does not teach the claimed thickness of the silicon nitride capping layer, because the language of claim 16, relied upon by the Examiner, only specifies a thickness for a silicon *dioxide* capping layer (Br. 16).

Appellants' argument is not persuasive of Examiner error. Guo teaches that the thickness of cap dielectric film 22 is kept to approximately between 100 Å to 500 Å (FF 6). Guo's teaching of thickness is not restricted to one particular material; Guo teaches that the cap dielectric film may be formed of silicon dioxide (FF 6).

Therefore, because Appellants have not identified error in the Examiner's position, we will sustain the Examiner's rejection of claim 16 under 35 U.S.C. § 102.

CLAIM 17

Appellants argue that Guo does not anticipate claim 17 because Guo does not specify a nitride sidewall deposited with a BTBAS precursor. Appellants' argument is not persuasive, because, as the Examiner notes, the gate stack of Guo includes a nitride sidewall (Fig. 4, element 16). In Appellants' view, because BTBAS includes a carbon-containing compound that affects transistor performance, one of ordinary skill would not have considered using a BTBAS precursor "unless it is proactively specified" (Br. 17).

Appellants' argument is not persuasive. The Examiner rejected this product-by-process claim over a prior art product that appears to be identical. The burden then shifted to Appellants to come forward with evidence establishing an unobvious difference between the claimed product and the prior art product. *Marosi,* 710 F.2d at 803. Appellants' argument regarding the use of BTBAS precursor amounts to an argument that one of ordinary skill in the art would not have practiced the same process as Appellants. It is *not* an argument that the claimed product differs in an unobvious way from the prior art product. Appellants have not presented any evidence tending to establish that difference.

Because Appellants did not demonstrate error in the Examiner's rejection of claim 17 under § 102, we will sustain the rejection.

CLAIM 13

Appellants argue that Guo does not render the claimed invention obvious, because Guo does not teach that the extension regions for the PMOS transistors have a dopant concentration in the range of about 1-2 e20 atoms/cm3, and that such a dopant concentration is not "notoriously well known in the art," as the Examiner found (Br. 18).

Appellants' arguments are not persuasive of Examiner error. We agree with the Examiner that Appellants have disclosed no criticality to or unexpected results flowing from the particular range of dopant concentration claimed (Ans. 14). We further agree with the Examiner that dopant concentrations corresponding to "lightly-doped" are well known in the art (Ans. 6), and that determining the optimum range of dopant concentration here would require no more than routine experimentation. *See Aller*, 220 F.2d at 456.

Accordingly, we conclude that Appellants have not demonstrated error in the Examiner's rejection, and we will sustain the § 103 rejection of claim 13.

CLAIM 14

Appellants argue that Guo does not render the claimed invention obvious, because Guo does not teach that the source and drain regions for the PMOS transistors have a dopant concentration in the range of about 1-2 e20 atoms/cm3, and that such a dopant concentration is not "notoriously well known in the art," as the Examiner found (Br. 19).

Appellants' arguments are not persuasive of Examiner error. We agree with the Examiner that Appellants have disclosed no criticality to or unexpected results flowing from the particular range of dopant concentration

claimed (Ans. 14). We further agree with the Examiner that appropriate dopant concentrations for source and drain regions are well known in the art (Ans. 6), and that determining the optimum range of dopant concentration here would require no more than routine experimentation. *See Aller*, 220 F.2d at 456.

Accordingly, we conclude that Appellants have not demonstrated error in the Examiner's rejection, and we will sustain the § 103 rejection of claim 14.

CLAIM 15

Appellants argue that Guo does not render the claimed invention obvious. Specifically, because Guo allegedly does not teach the interfacial nitride layer recited in parent claim 11, Guo therefore also does not teach the claimed concentration range of atomic nitrogen (Br. 20).

This argument is not considered persuasive, because as noted *supra*, we find that Guo does teach the interfacial nitride layer recited in claim 11. In the absence of any separate argument for the patentability of claim 15, then, we do not find error in the Examiner's rejection of claim 15 under § 103, for the same reasons expressed with respect to the § 102 rejection of claim 11, *supra*.

CLAIM 18

Appellants present the same arguments for the various elements of claim 18 (i.e., that Guo does not teach a layer of silicon oxide over the total exposed surface of the lightly-doped extension regions; that Guo does not teach an interfacial layer of nitrogen; that elements 14 and 16 of Guo cannot anticipate all of the conductive structure of the gate stack, the oxide sidewall, and the interfacial layer of nitrogen; and that Guo does not teach a

capping layer of silicon nitride of the appropriate thickness) that were presented in favor of the patentability of claims 11 and 16. As noted *supra*, we find that Guo teaches all of the elements of claims 11 and 16. We therefore find that Guo teaches all of the analogous elements of claim 18. Accordingly, we will sustain the § 103 rejection of claim 18 for the same reasons given supra for sustaining the § 102 rejection of claims 11 and 16.

CONCLUSIONS OF LAW

1. Appellants have not shown that the Examiner erred in finding that Guo teaches: a layer of insulating material, composed of silicon oxide, over a total exposed surface of the lightly-doped extension regions; an interfacial layer of nitrogen formed at the interface of the lightly-doped extension regions and the layer of insulating material; a capping layer of contiguous silicon nitride having a thickness of 200-1000 angstroms; and a gate stack having a nitride sidewall deposited with a BTBAS precursor, as the claims require.

2. Appellants have not shown that the Examiner erred in finding that it would have been obvious to modify Guo to provide extension regions and source and drain regions with the dopant concentration claimed, or that the interfacial nitride layer should have an atomic nitrogen concentration in the range of 2-15 atomic percent.

ORDER

The Examiner's rejection of claims 11-18 is affirmed.

No time period for taking any subsequent action in connection with this appeal may be extended under 37 C.F.R. § 1.136(a)(1)(iv).

AFFIRMED

ELD

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